Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented) A method of designing an integrated circuit having digital and analog circuit portions, said digital and analog circuit portions each having defined functions, comprising:

providing an emulation circuit, which is capable of generating noise, and which has a configuration capable of being modified;

affixing said emulation circuit on a test substrate;

providing a version of said analog circuit portion having at least some of said defined functions of said analog circuit portion;

affixing said analog circuit version on said test substrate;

testing said analog circuit version while modifying the configuration of the emulation circuit; and

providing the digital circuit portion, the design of which is based on the testing of the analog circuit version while modifying the configuration of the emulation circuit.

Claim 2 (original) The method of claim 1 further comprising modifying said analog portion in response to said testing step.

Claim 3 (previously presented) The method of claim 2 further compromising:

repeating said affixing emulation circuit step, said analog circuit portion providing step, said analog circuit portion version affixing step and said analog circuit portion version testing step so that a version of said analog circuit portion having all of said defined functions of said analog circuit portion, with acceptable response to said noise effects under operating conditions is obtained.

Claim 4 (original) The method of claim 1 further comprising:

providing a version of said digital circuit portion having all of said defined functions of said digital circuit portion; and

affixing said digital circuit portion version to an integrated circuit including said version of said analog circuit portion having all of said defined functions of said analog circuit portion, with acceptable response to said noise effects under operating conditions.

Claim 5 (original) The method of claim 4 wherein said digital circuit portion providing step includes testing said defined functions of said digital circuit portion separately from said analog circuit portion.

Claim 6 (original) The method of claim 5 wherein said digital circuit portion testing includes programming an FPGA for testing said defined functions of said digital circuit portion.

Claim 7 (original) The method of claim 5 wherein said digital circuit portion testing includes simulating said defined functions of said digital circuit portion.

Claim 8 (original) The method of claim 1 wherein said emulation circuit comprises at least one array comprising at least one shift register.

Claim 9 (original) The method of claim 8, wherein said testing said analog circuit version is performed while alternately shutting off and turning on at least one array.

Claim 10 (original) The method of claim 8, wherein said shift register comprises:

a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit; and

a plurality of interconnecting logic blocks, wherein said plurality of flip-flops couple to each other through said plurality of interconnecting logic blocks sequentially, and wherein said data bits form a data pattern.

Claim 11 (original) The method of claim 10, wherein said testing said analog circuit version is performed while applying a signal at said clock input.

Claim 12 (original) The method of claim 11, wherein said testing said analog circuit version is performed while varying said clock input signal.

Claim 13 (original) The method of claim 10 wherein said testing said analog circuit version is performed while varying said data pattern.

Claim 14 (original) The method of claim 10, wherein said interconnecting logic blocks comprise Exclusive-Or gates, and wherein said testing said analog circuit version is performed while varying said data pattern using said Exclusive-Or gates.

Claim 15 (original) The method of claim 10, wherein said interconnecting blocks comprise a plurality of logic paths, wherein each logic path is comprised of differing amounts of logic gates, and wherein said testing of said analog circuit portion is performed while alternately selecting from among said plurality of logic paths.

Claim 16 (original) The method of claim 10, wherein at least one of said flip-flops is coupled to an equal number of pads through an equal number of output drivers, which may be enabled and disabled.

Claim 17 (original) The method of claim 16, wherein said testing of said analog circuit portion is performed while enabling and disabling said output drivers.

Claim 18 (original) The method of claim 1 wherein said analog circuit portion includes an RF circuit subportion.

Claim 19 (original) The method of claim 1, wherein a number of gates in said emulation circuit is substantially equivalent to a number of gates in said digital circuit portion.

Claims 20-30 (cancelled)

Claim 31 (previously presented) A method of designing an integrated circuit having digital and analog circuit portions, said digital and analog circuit portions each having defined functions, comprising:

providing an emulation circuit, which is capable of generating noise, and which comprises a plurality of logic circuits;

affixing said emulation circuit on said integrated circuit;

providing a version of said analog circuit portion having at least some of the defined functions of said analog circuit portion;

affixing said analog circuit version on said integrated circuit;

testing said analog circuit version,

providing said digital circuit portion, wherein said digital circuit portion may be formed by rewiring said emulation circuit.

Claim 32 (original) The method of claim 31 further comprising modifying said analog portion in response to said testing.

Claim 33 (previously presented) The method of claim 32 further compromising:

repeating said affixing emulation circuit step, said analog circuit portion providing step, said analog circuit portion version affixing step and said analog circuit portion version testing step so that a version of said analog circuit portion having all of said defined functions of said analog circuit portion, with acceptable response to said noise effects under operating conditions is obtained.

Claim 34 (previously presented) The method of claim 31 further comprising reconnecting said logic circuits to provide for said digital portion.

Claim 35 (previously presented) The method of claim 31, wherein said noise generated by said emulation circuit is substantially equivalent to noise generated by said digital circuit portion.

Claim 36 (previously presented) An integrated circuit having digital and analog portions, designed by a process comprising:

providing an emulation circuit, which generates noise, and which comprises a circuit path that may be modified;

affixing said emulator circuit on a test substrate;

providing a version of said analog circuit portion having at least some of said defined functions of said analog circuit portion;

affixing said analog circuit version on said test substrate;

testing said analog circuit version while modifying the circuit path in the emulation circuit; and

providing the digital portion, the digital portion having a configuration based on the testing of the analog circuit while modifying the circuit path in the emulation circuit.

Claim 37 (original) The integrated circuit of claim 36, designed by a process further comprising modifying said analog portion in response to said testing step.

Claim 38 (previously presented) The integrated circuit of claim 37, designed by a process further compromising:

repeating said affixing emulation circuit step, said analog circuit portion providing step, said analog circuit portion version affixing step and said analog circuit portion version testing step so that a version of said analog circuit portion having all of said defined

functions of said analog circuit portion, with acceptable response to said noise effects under operating conditions is obtained.

Claim 39 (original) The integrated circuit of claim 36, designed by a process further comprising:

providing a version of said digital circuit portion having all of said defined functions of said digital circuit portion; and

affixing said digital circuit portion version to an integrated circuit including said version of said analog circuit portion having all of said defined functions of said analog circuit portion, with acceptable response to said noise effects under operating conditions.

Claim 40 (original) The integrated circuit of claim 36 wherein said emulation circuit has at least one array comprising at least one shift register.

Claim 41 (original) The integrated circuit of claim 40, wherein said shift register comprises:

a plurality of flip-flops, each having a clock input for receiving a clock input signal, and each storing a data bit; and

a plurality of interconnecting logic blocks, wherein said plurality of flip-flops couple to each other through said plurality of interconnecting logic blocks sequentially, and wherein said data bits form a data pattern.

Claim 42 (original) The integrated circuit of claim 36 wherein said analog circuit portion includes an RF circuit subportion.

Claim 43 (original) The integrated circuit of claim 36, wherein a number of gates in said emulation circuit is substantially equivalent to a number of gates in said digital circuit portion.